

Fig. 1 PRIOR ART

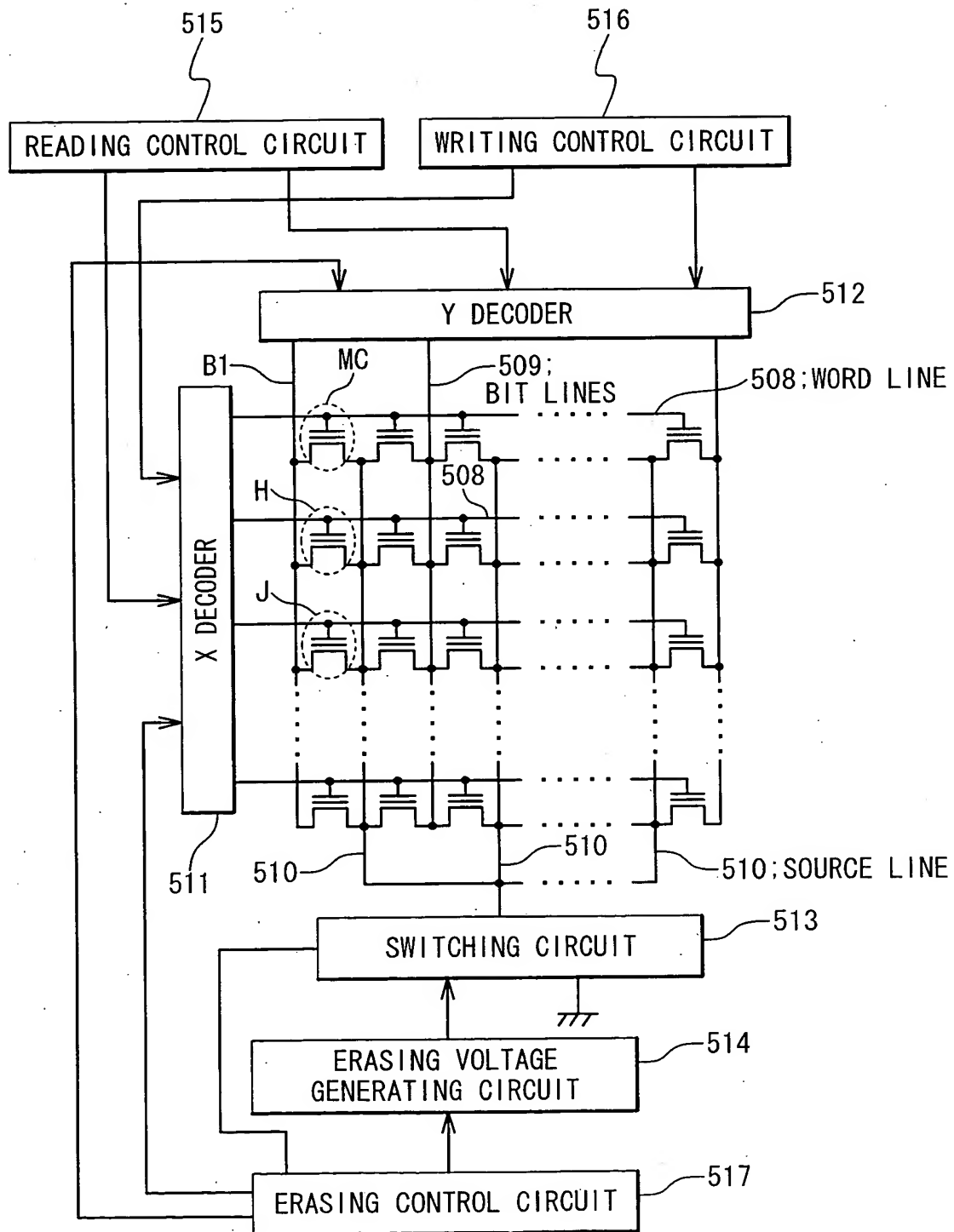


Fig. 2A PRIOR ART

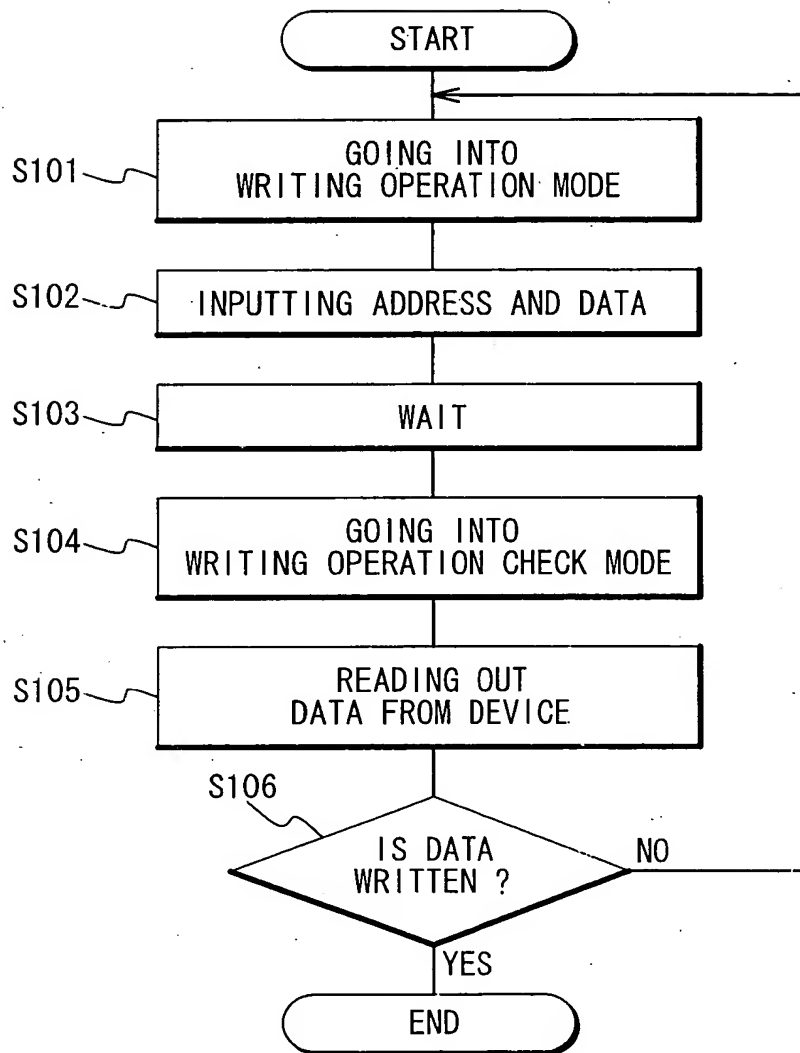


Fig. 2B PRIOR ART

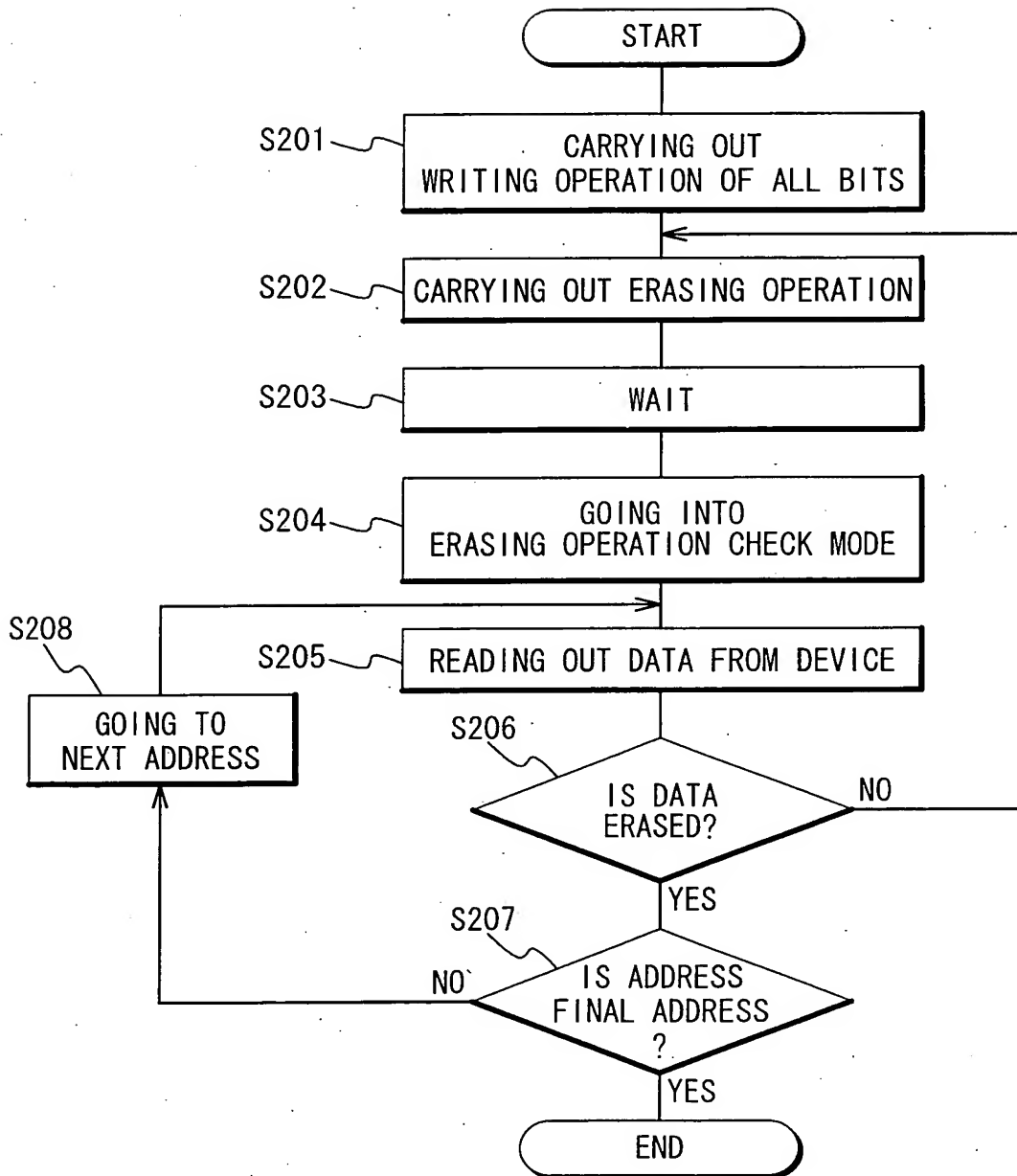


Fig. 3 PRIOR ART

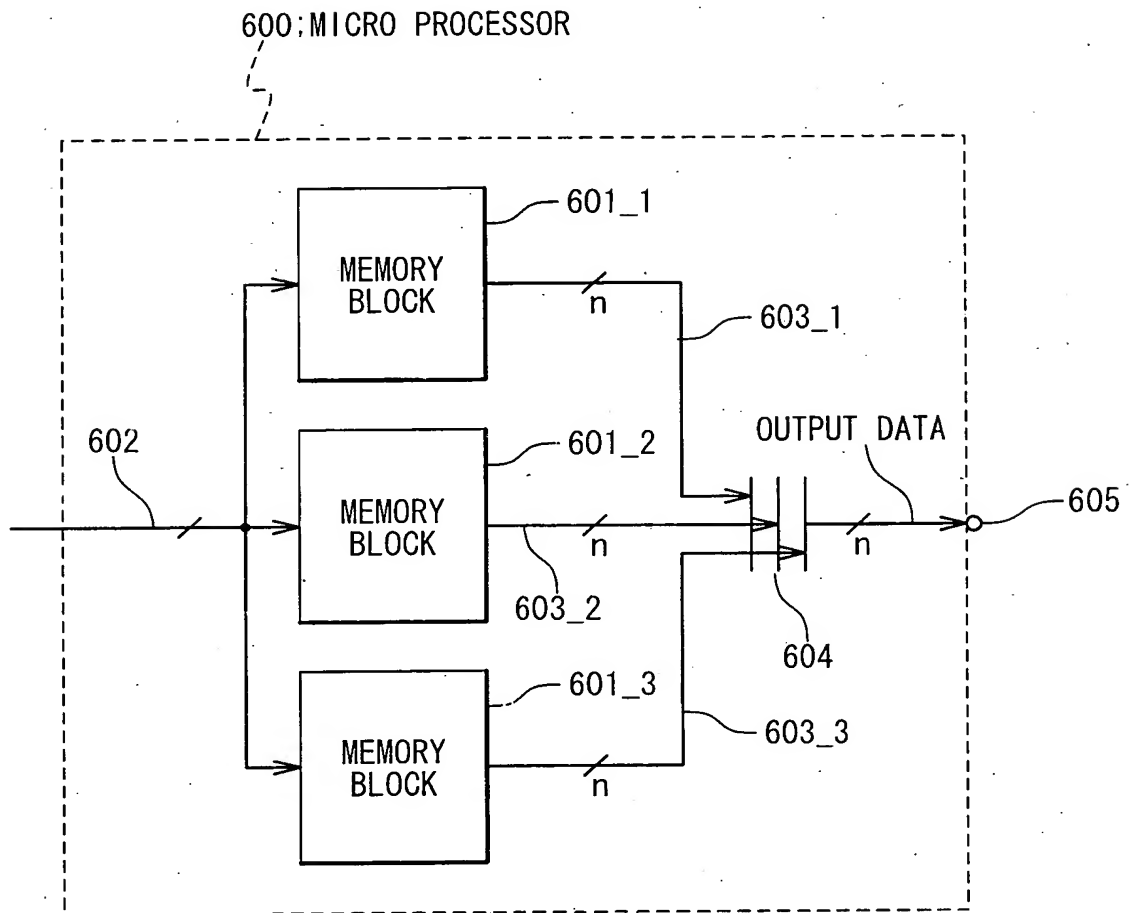
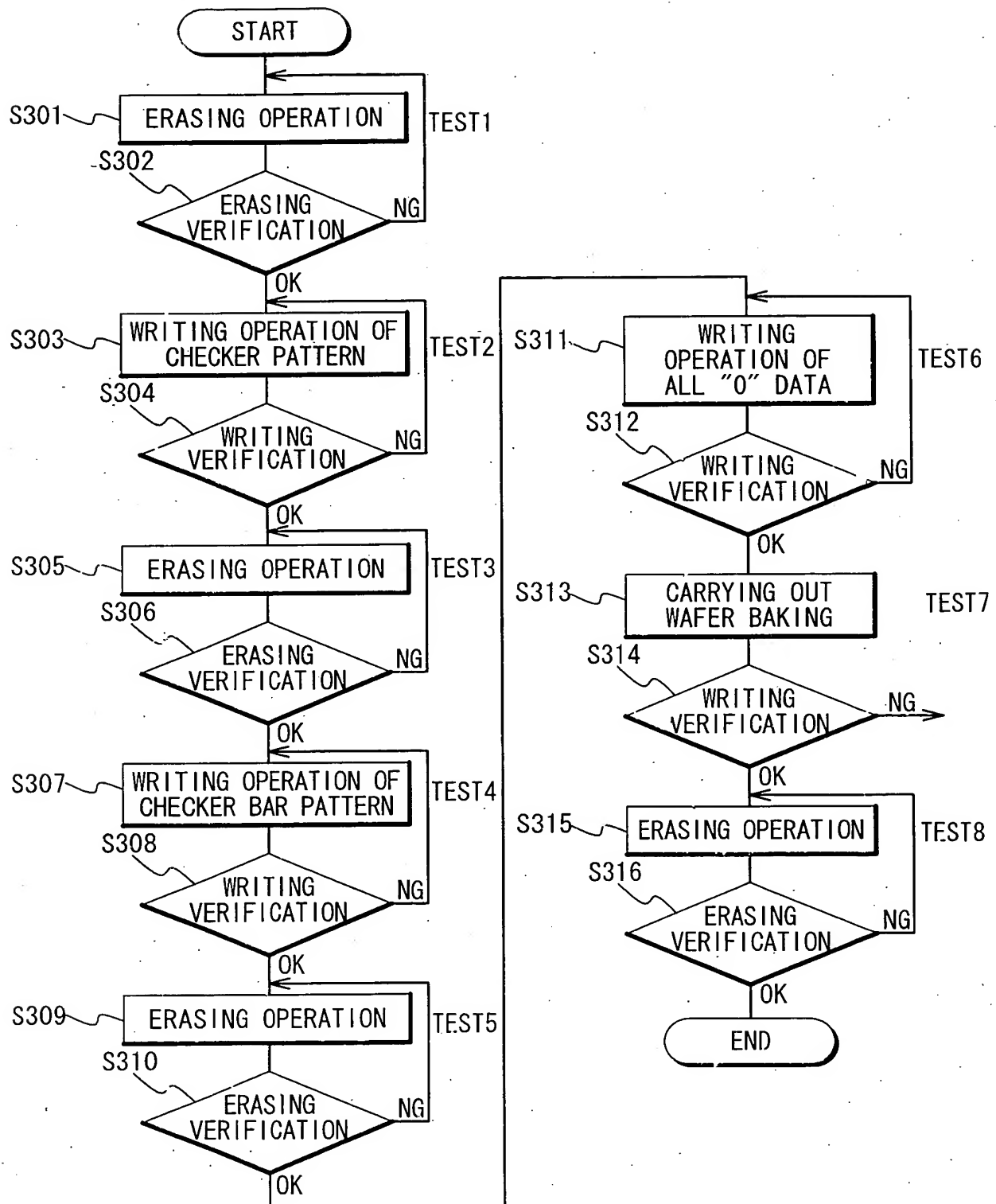


Fig. 4 PRIOR ART



700:LSI Fig. 5A PRIOR ART

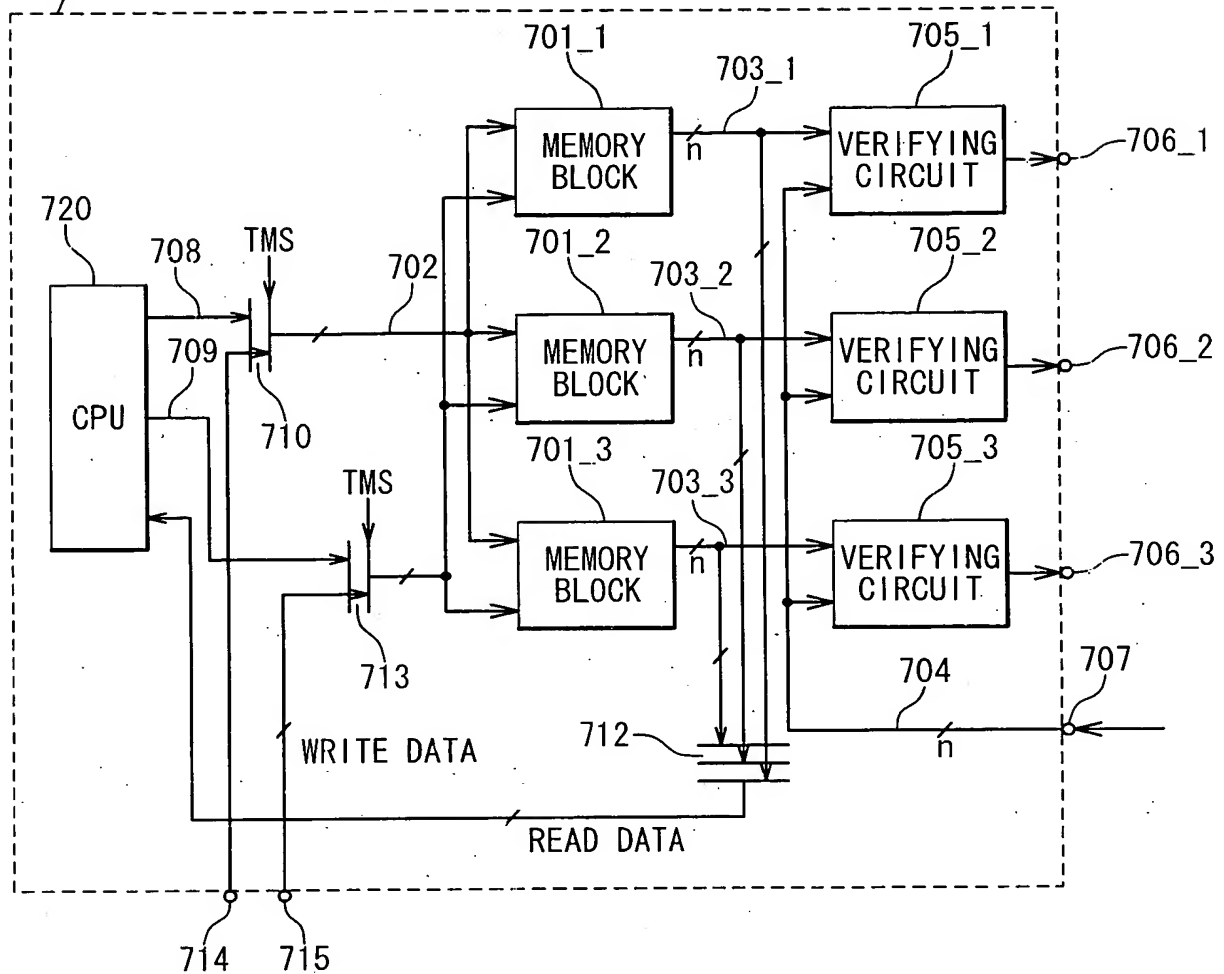


Fig. 5B PRIOR ART

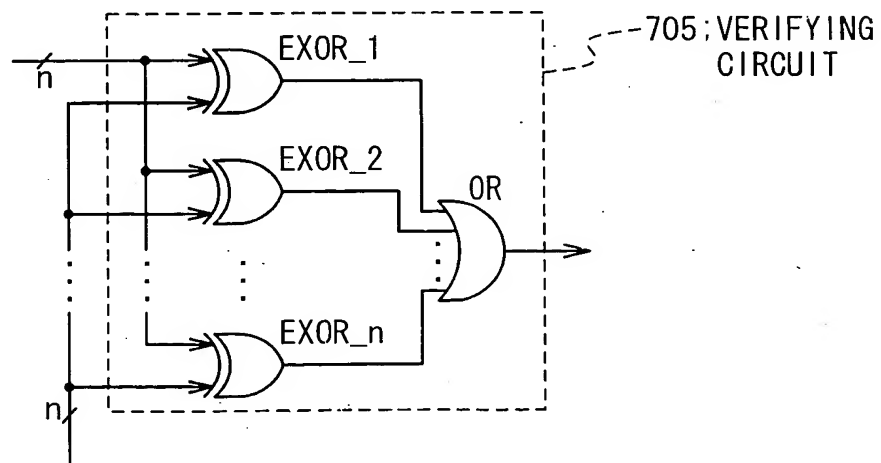


Fig. 6A

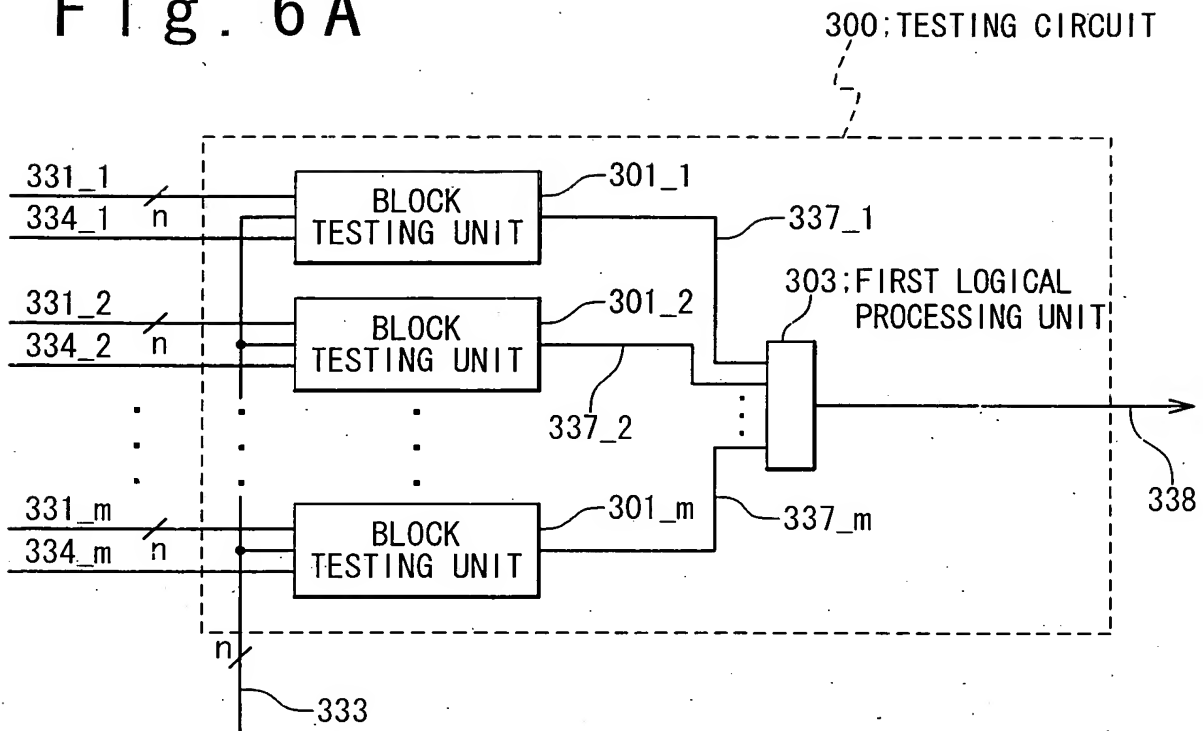


Fig. 6B

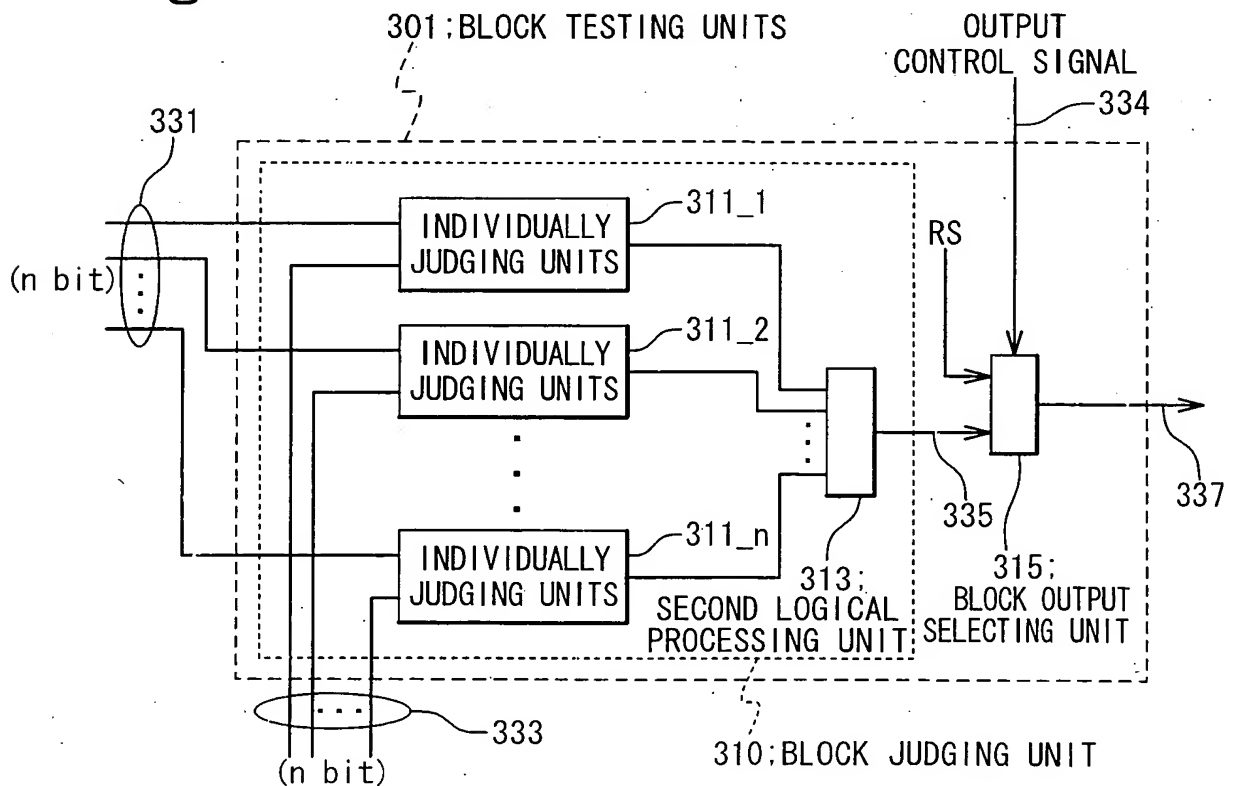


Fig. 7

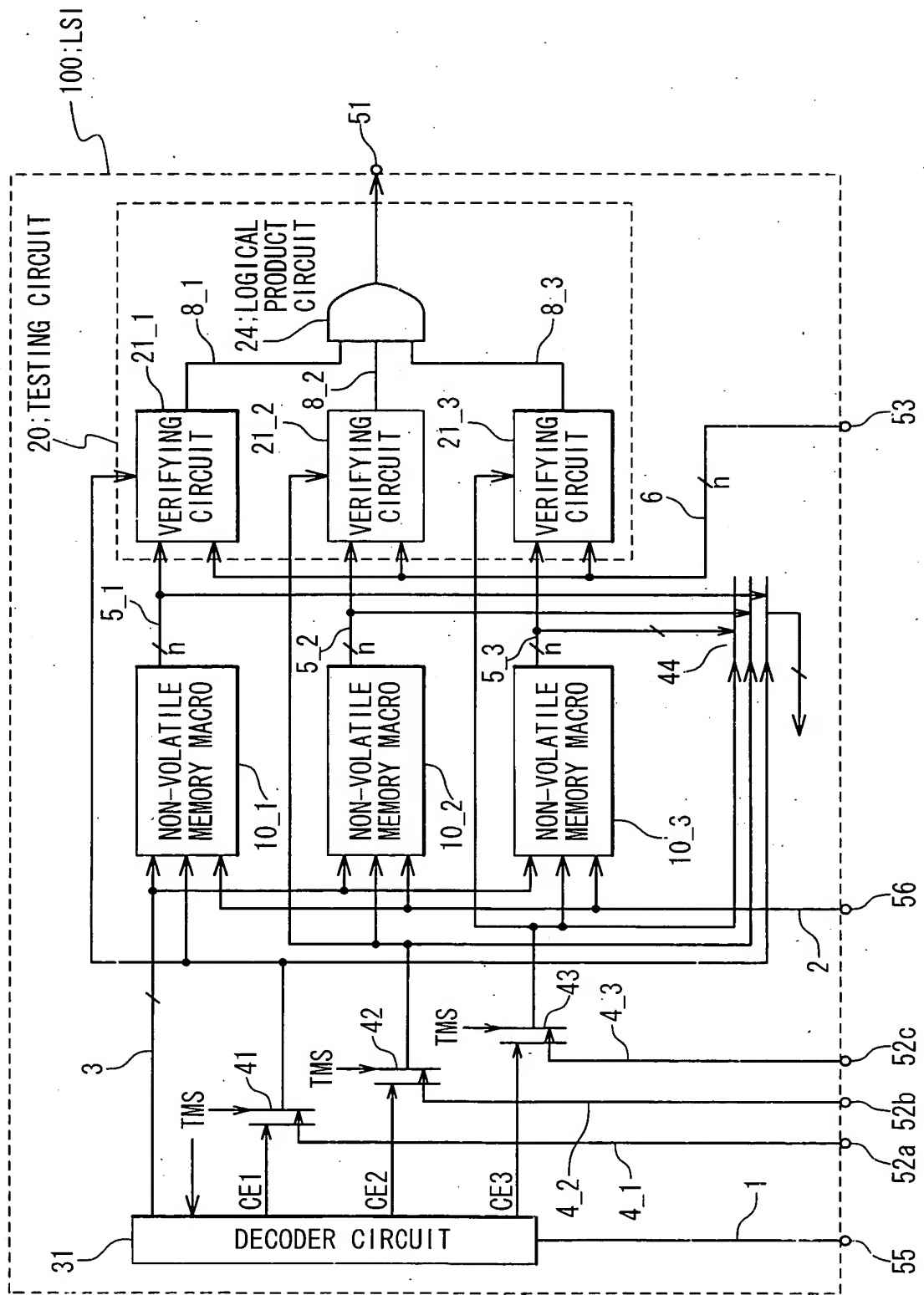


Fig. 8

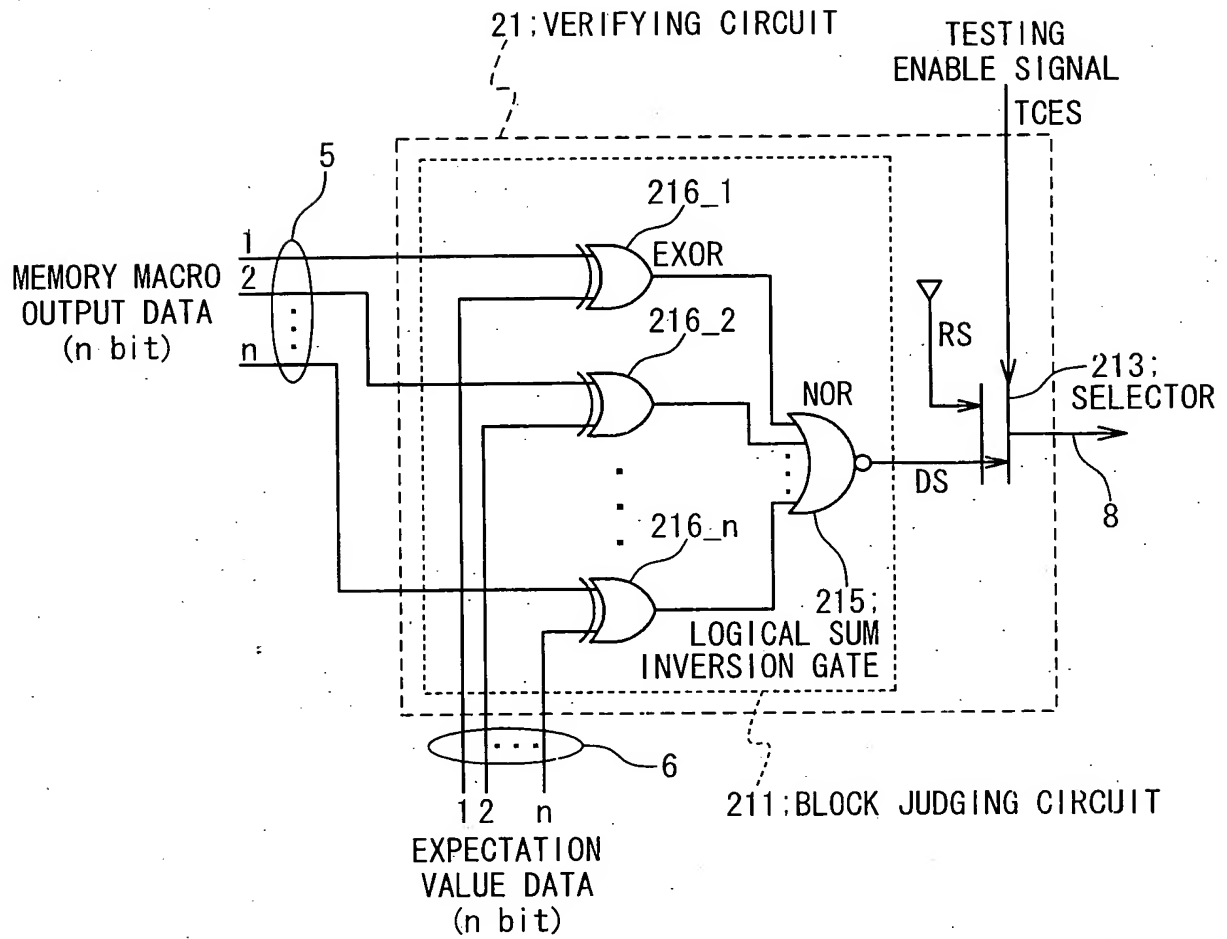


Fig. 9A

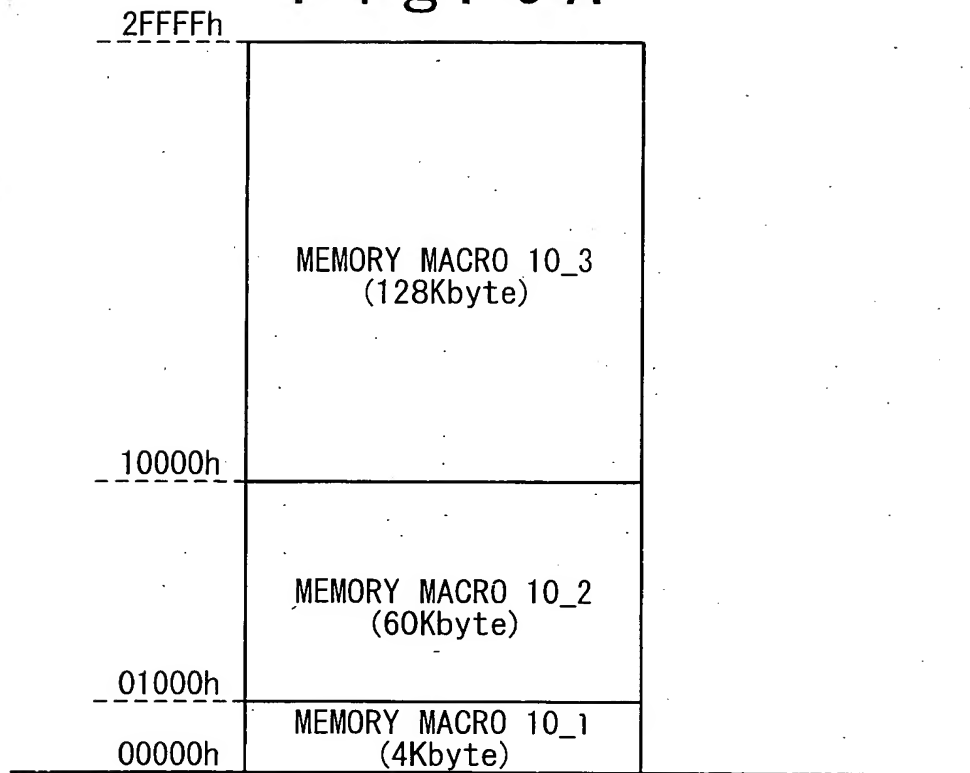


Fig. 9B

		FIRST SECOND	OUTPUT OF DECODE CIRCUIT			
			CE3	CE2	CE1	SECOND ADDRESS
MEMORY MACRO 10_3	FINAL ADDRESS	2FFFFh	1	0	0	1FFFFh
	START ADDRESS	10000h				00000h
MEMORY MACRO 10_2	FINAL ADDRESS	0FFFFh	0	1	0	0EFFFh
	START ADDRESS	01000h				00000h
MEMORY MACRO 10_1	FINAL ADDRESS	00FFFh	0	0	1	00FFFh
	START ADDRESS	00000h				00000h

Fig. 10A

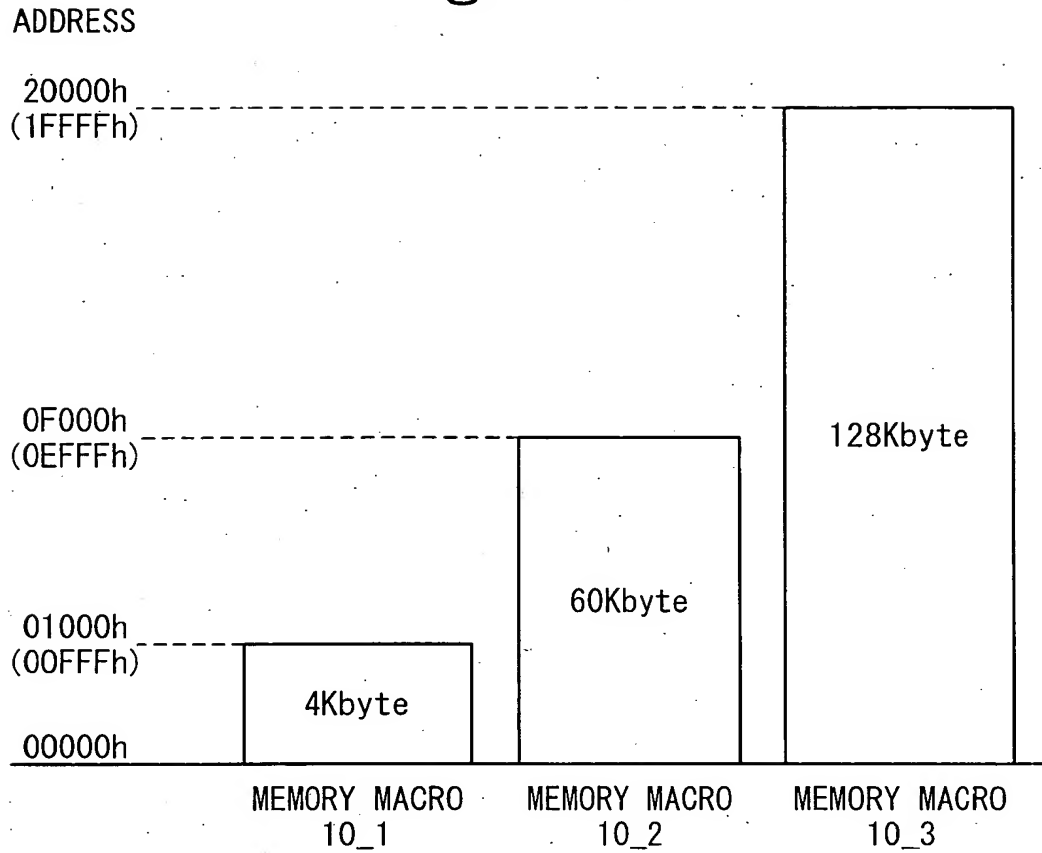


Fig. 10B

ADDRESS	00000h ~00FFFh	01000h ~0EFFFh	0F000h ~1FFFFh
TCES4_1	1	0	0
TCES4_2	1	1	0
TCES4_3	1	1	1

Fig. 11

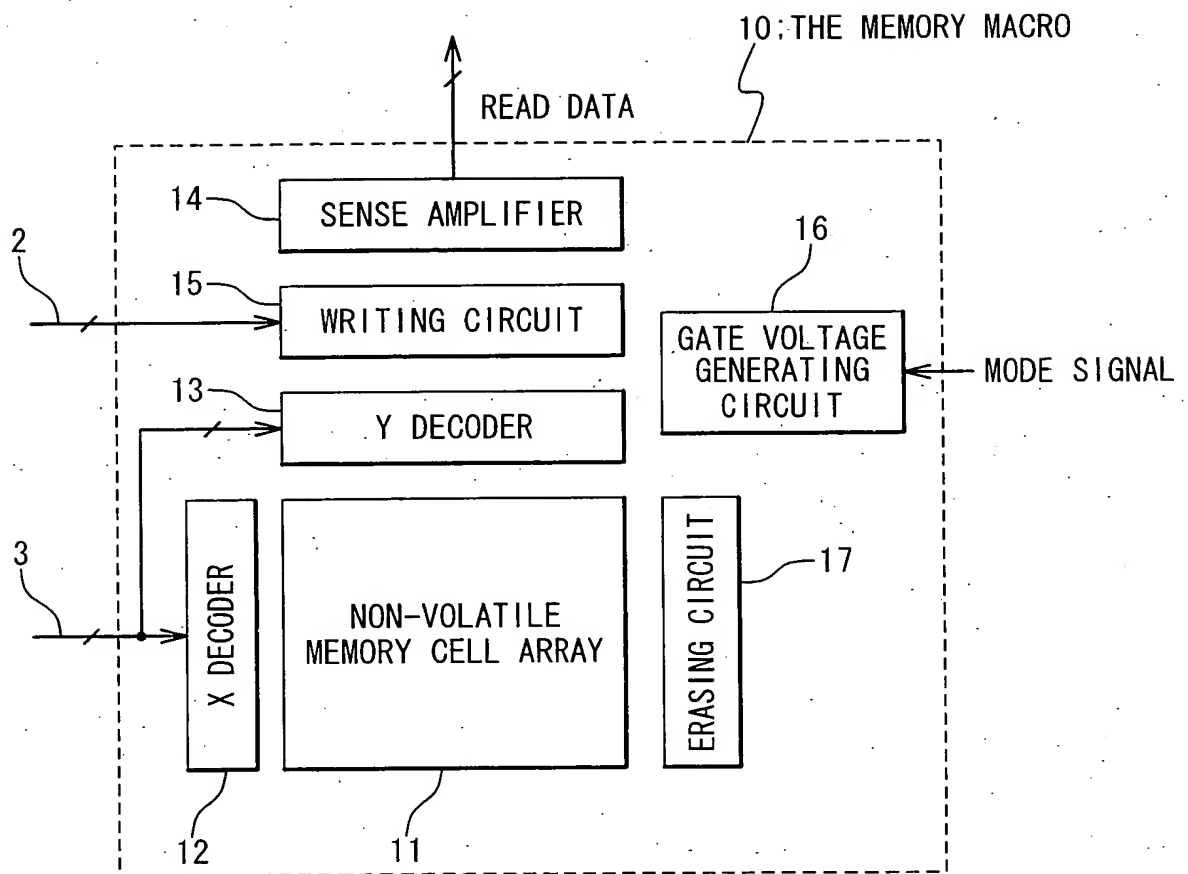


Fig. 12A

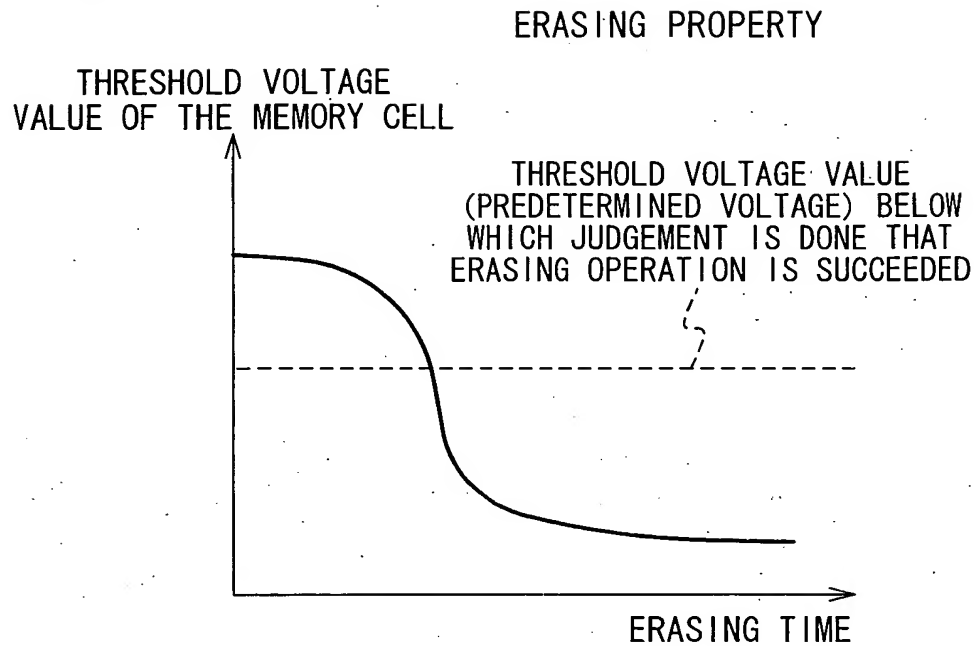
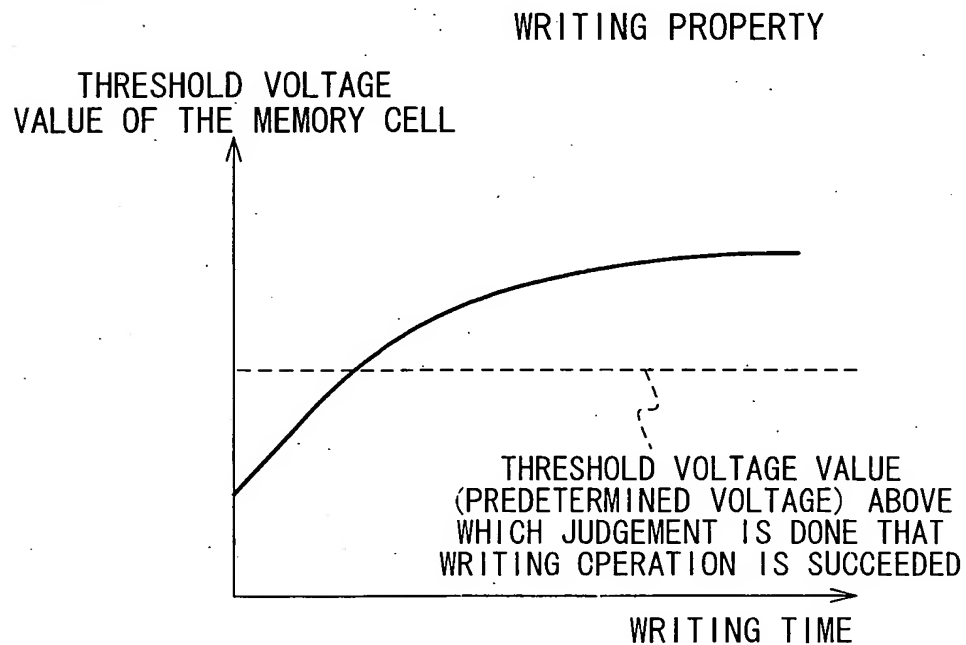
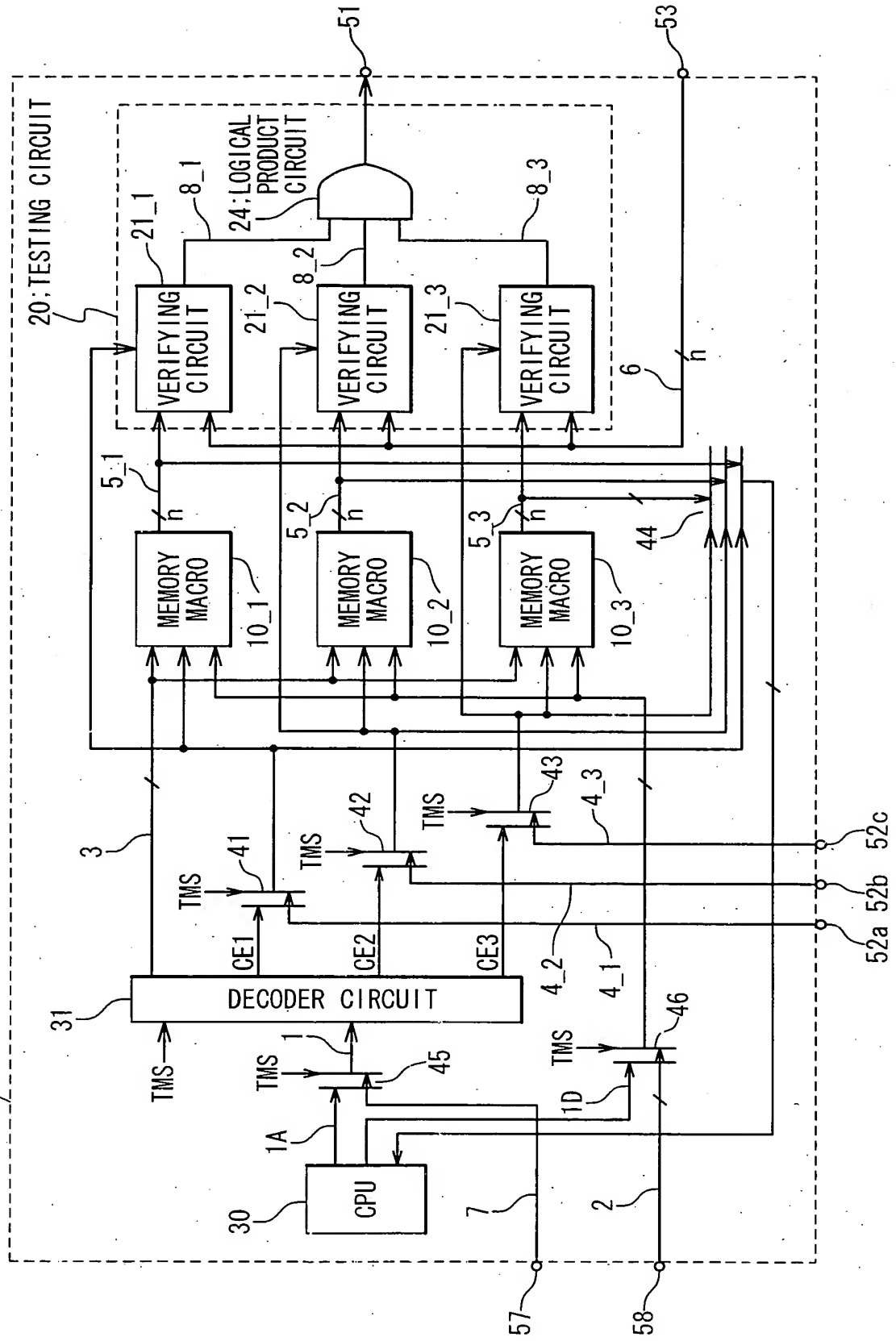


Fig. 12B



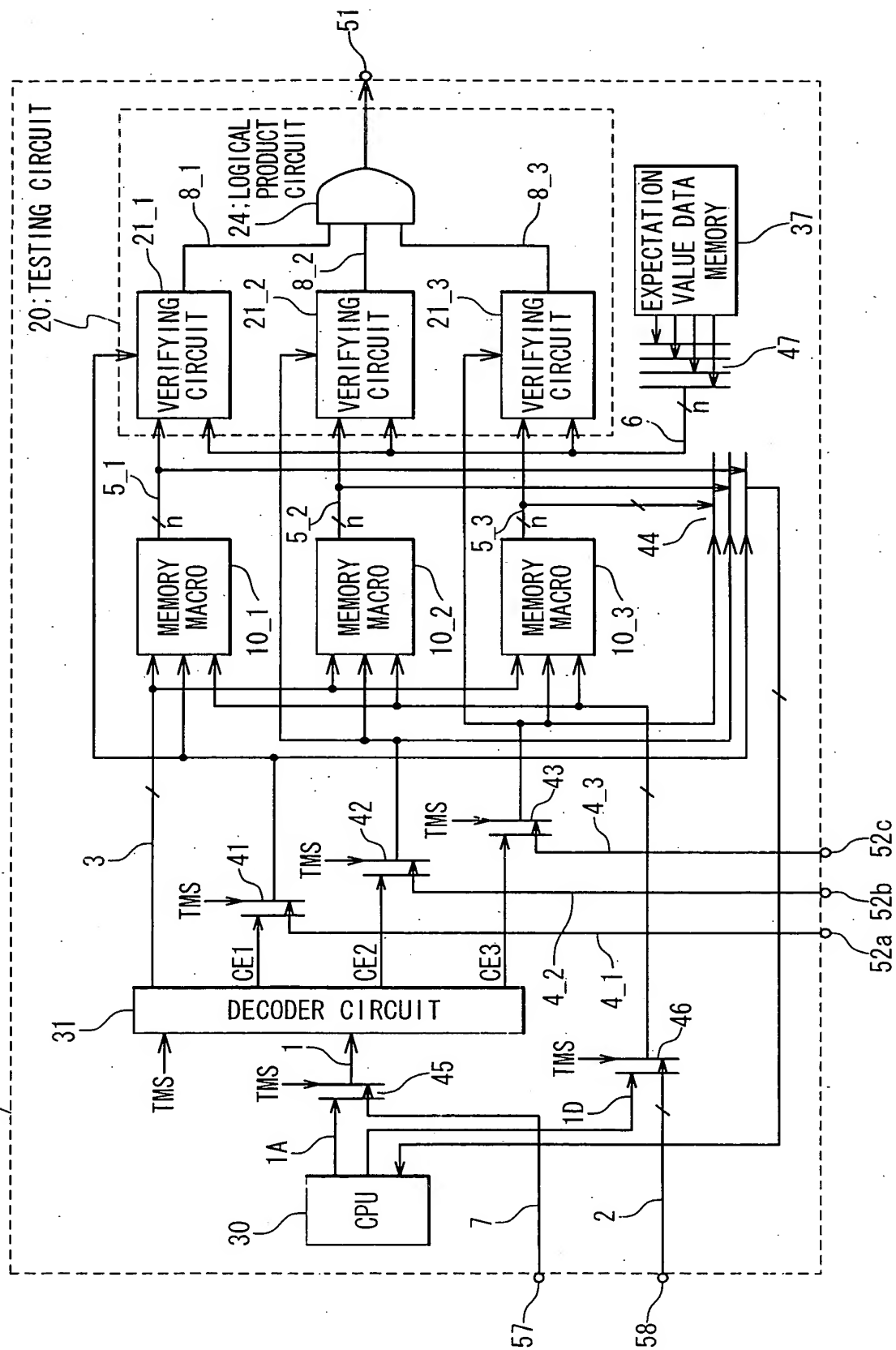
100A:LSI

Fig. 13



100B:LSI

Fig. 14



100C:LSI

Fig. 15

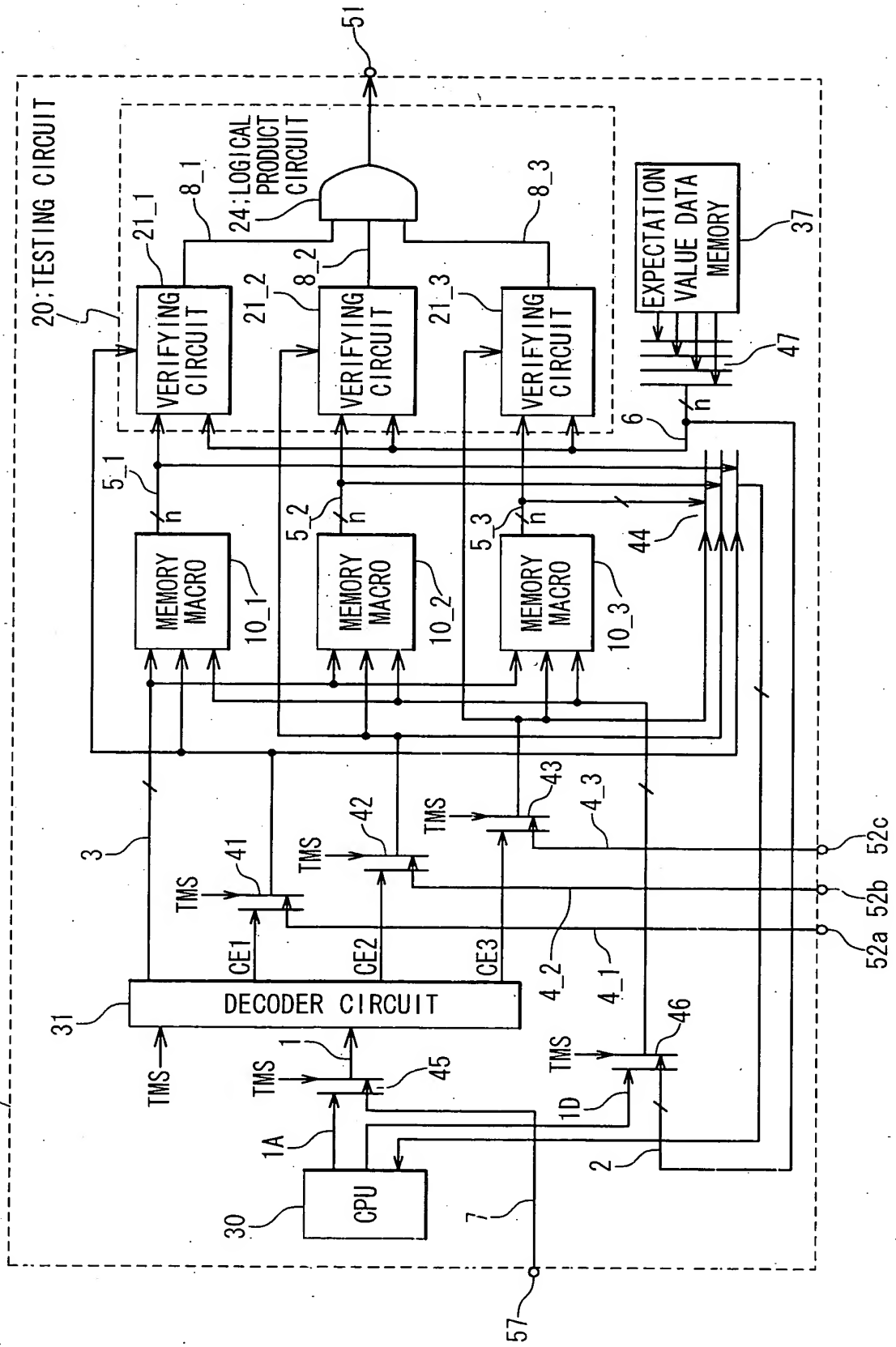


Fig. 16

